L-BAND HIGH POWER TRANSMIT/RECEIVE MODULE FOR ELECTRONICALLY SCANNED CYLINDRICAL ARRAY RADAR

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ABSTRACT

This paper presents the development of an L-band solid-state transmit/receive (T/R) module operating over 1.2 - 1.4 GHz for an electronically scanned array radar. Silicon (Si) bipolar transistors are used in the high power amplifier in the transmit channel and GaAs FETs are used for the low-noise amplifier in the receive channel. Key performance parameters of the T/R module are an average output power of >280W peak, (100μs pulse width, 10% duty cycle) reflecting a gain of 23.5dB, noise figure of <2.8dB (LNA N.F. <1.2dB), receive gain of >32.5dB, and MTI improvement factor of 70dBc (pulse-to-pulse stability).

INTRODUCTION

The increasingly complex threat environment for target detection radars has driven system architects to the use of electronically steerable active aperture antenna arrays. Transmit/Receive modules are key elements in any active antenna array.

An L-band solid-state transmit/receive module is developed for an unattended electronically scanned cylindrical array radar. Silicon (Si) bipolar transistors have high power microwave amplification characteristics which enable new system concepts that could not be brought to fruition without this technology. Si bipolar transistors operating in efficient class C mode are used to generate peak output power of 400W in the transmit channel. Low-noise GaAs MESFETs are used in the Low-noise amplifier (LNA) in the receive channel and Si PIN diodes having >800V breakdown voltage are used for the high and low power switching networks in the transmit and receive channels.

The T/R module results presented in this paper represent the state-of-the-art performance for a solid-state electronically scanned array radar. The T/R module development has been successfully transferred to production.

This work was performed on the AN/FPS-124 system under Contract No. F19628-89C-0058 for the US Air Force

TRANSMIT/RECEIVE MODULE DESIGN

The T/R module is designed to operate over the frequency range 1.2 - 1.4 GHz and the temperature range 0°C to 30°C. The transmit channel requirements include an output power of >227-W at 95μs pulse width and 10% duty cycle, and unit-to-unit gain and phase tracking of <0.5dB and 20°RMS, respectively. Waveform characteristics such as rise time, amplitude droop, and phase linearity are other critical requirements, which are listed in Table 3 in the performance section. Receive channel gain requirements are a gain of >32dB and a maximum noise figure of 3.5dB, and unit-to-unit gain and phase tracking of 0.46dB and 5.4°RMS, respectively. Transmit and receive pulse-to-pulse stability (MTI improvement factor) of 70dBc is a critical requirement. The T/R module is designed to operate in an unattended radar, having high reliability and fault monitoring features.

A block diagram of the T/R module is shown in Fig. 1. The module consists of three subassemblies: a) High Power Amplifier (HPA); b) Low Noise Amplifier (LNA)/Switch and c) control/performance monitoring electronics, which together produce RF amplification, provide required transmit-power to the antenna element, provide a path for received signal to return from the antenna to the receiver, allow sector and beam switching, and perform PM/FI functions. The photograph of the complete T/R module is shown in Fig. 2.

The RF input signal of 1.25W peak, on transmit, passes through a low power T/R switch, four stages of high power amplification in the HPA assembly, a circulator, a directional detector which monitors HPA output power, a high power T/R switch, sector switch, a beam switch (all switches are in the LNA/Switch

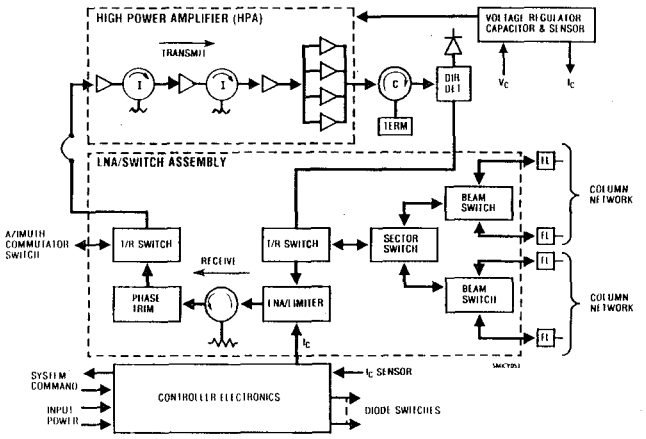

Fig. 1. Block Diagram of T/R Module

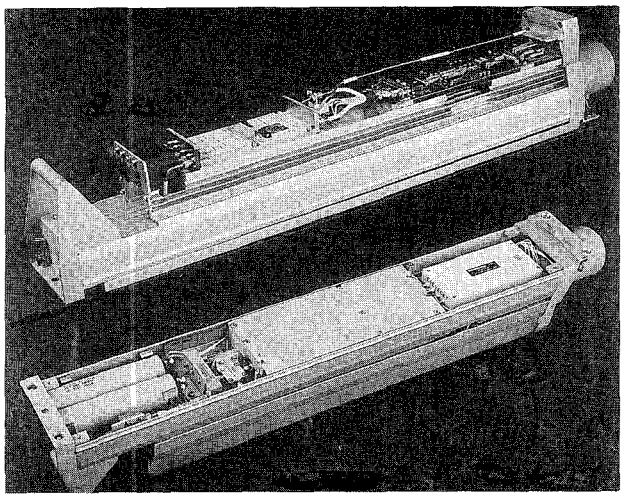

Fig. 2. Photograph of Complete T/R Module Assembly

assembly) and a band-pass filter to the column network/antenna element. The receive signal passes from the antenna element through a band-pass filter, beam switch, sector switch, high power T/R switch, receive/protect circuitry (limiter), three stages of low noise amplification, isolator, receive phase compensation circuit and low power T/R switch in the LNA/Switch Assembly, to the receiver. The control electronics assembly provides the DC bias signals, control signals for switches, and a performance monitoring/fault indicating (PM/FI) function.

HIGH POWER AMPLIFIER DESIGN

A schematic and a layout of the HPA are shown in Figs. 3 and 4, respectively. The HPA consists of four stages which amplify a 1-W signal to a 400-W output signal. HPA performance is maintained over a wide input power dynamic range of 3.5dB. This feature is essential in an active aperture radar to accomodate RMS amplitude errors in the distribution and switching networks. Si bipolor transistors are used for amplification. The first stage is designed to supply 5.5-W output power with a gain of 7.4 dB. The second stage provides at least 27W output power with a gain of 6.9 dB, followed by a third stage having a gain of 6.7 dB and output power of 125W. The final stage consists of four paralleled 110W transistor stages with minimum gain of 6.1dB, using Wilkinson power divider/combiner networks. Isolators are used for interstage buffering. The Wilkinson divider/combiner uses extra quarter wavelength sections to isolate the fourth from the third stage. Fixed attenuators are used between the first and second and second and third stages to prevent the following stages from being overdriven.

Each amplifier stage is designed to operate in class C mode to achieve high efficiency. Performance of the HPA is presented in Table 1. The data represents an average performance of approximately the first 500 HPAs built during the early production phase of the program. The average output power of >400W peak is achieved simultaneously with realization of the pulse fidelity (including phase across the pulse, phase linearity, amplitude droop, rise time), a maximum transistor junction temperature of <135°C, and maintaining the spurious signals and pushing factor such that pulse-to-pulse stability requirements are met at the T/R level.

LNA/SWITCH DESIGN

A schematic diagram and a photograph of the LNA/Switch assembly are shown in Figs. 5 and 6, respectively. The Low-Noise Amplifier (LNA)/Limiter consists of three stages of low-noise amplification using GaAs low-noise FETs and a diode limiter to protect the LNA up to 200 watts of input power. The LNA/Limiter achieves a gain of >36dB and a noise figure <1.2dB.

All SPDT switches shown in Fig. 5 utilize a Si PIN diode cerma chip, developed in a special mount, having the following characteristics:

Package insertion loss:	0.05 dB
Breakdown Voltage:	800V
Junction Capacitance:	0.4 pF
Series Resistance:	0.70 ohms,max.
Minority Carrier Lifetime:	3μsec

The above diode characteristics are selected to achieve the power handling capability of > 400 W looking into a

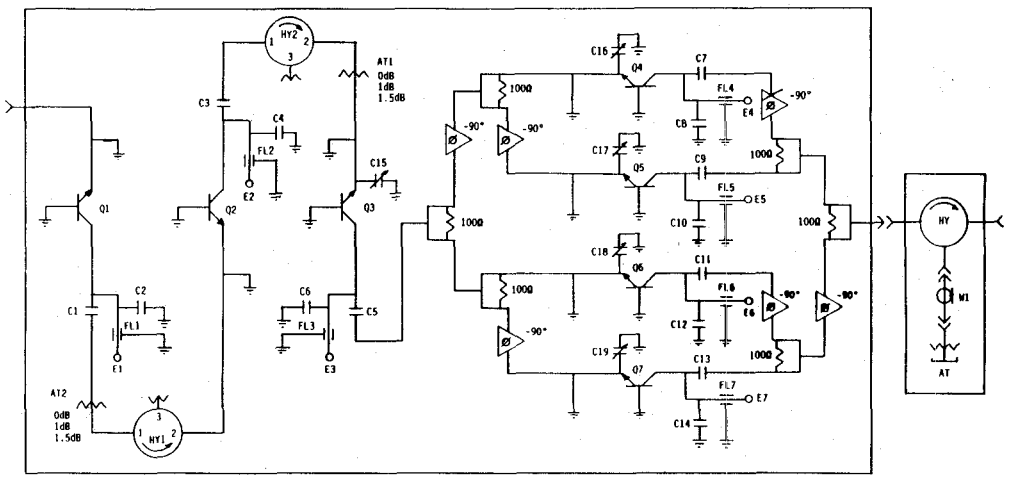

Fig. 3. Schematic of High Power Amplifier

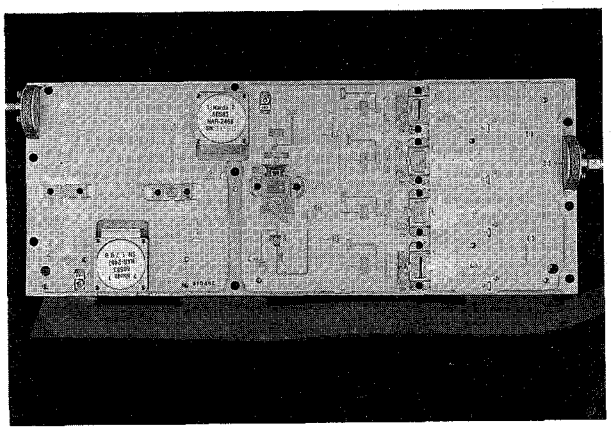

Fig. 4. Photograph of High Power Amplifier Assembly

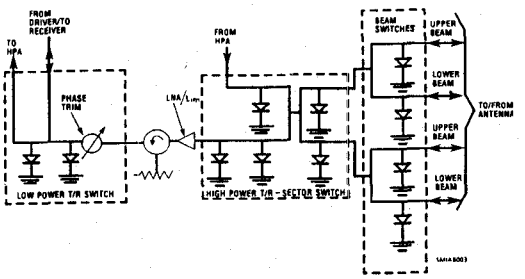

Fig. 5. Schematic of LNA/Switch with its Associated Sub-Circuit

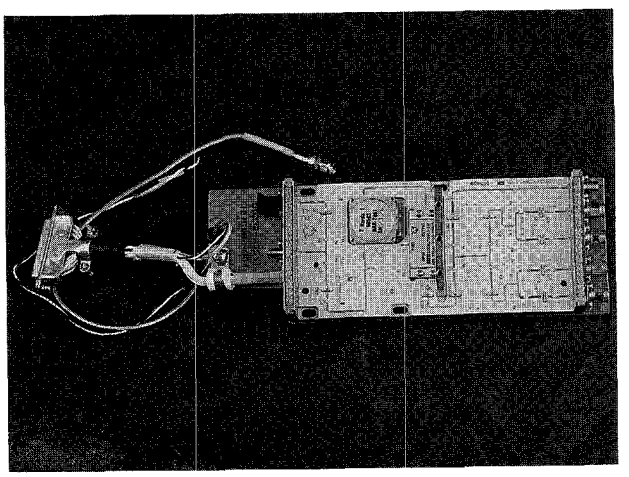

Fig. 6. Photograph of LNA/Switch Assembly

reflection coefficient of 1.0. The design of the switches utilizes a shunt diode configuration spaced a quarter wavelength from the switch junction to achieve low-loss, good match and high isolation. The Bias circuit design aids matching of the switch junction to reduce the mismatch loss of the three junctions in series. A hermetic Si PIN diode cerma chip is mounted on a gold plated post with a gold ribbon attached across the anode. This assembly provides high performance, small size and low cost as compared to the standard hermetic package diode. Performance of the LNA/Switch assembly is presented in Table 2. The data presented in Table 2 represents an average performance of approximately the first 500 units built during early production phase of the program.

CONTROL ELECTRONICS ASSEMBLY

The Control Electronics links the Beam Steering Unit (BSU) to the T/R module by reacting to the commands of the BSU. It drives the switch diodes and monitors the HPA output, regulator voltage and LNA current. It also tests every diode for failure, tests its own BIT, and supplies all results to the BSU.

FABRICATION

HPA and LNA/Switch assemblies are fabricated on a high dielectric (Er=10.5) soft substrate material backed by a thick metal plate, forming a single laminate. A cost effective batch fabrication process is developed using a vapor phase soldering technique. In this technique most of the components are soldered simultaneously onto the laminate, at precisely controlled temperature. Special fixtures and tooling are developed to hold all components to the laminate during the soldering operation.

The T/R module consists of an integral cold plate/housing assembly. The HPA and LNA/Switch subassemblies share a common air cooled heat sink, which reduces the overall cost, improves cooling efficiency and maintains low transistor junction temperature.

T/R MODULE PERFORMANCE

Electrical performance of the T/R module are presented in Table 3. The performance presented is an average of about 500 T/R modules, representing early production phase. T/R modules are fully characterized and the performance requirements have been met or exceeded.

CONCLUSIONS

A development of a solid-state T/R module using state-of-the-art Si bipolar power transistors has been presented. The development of the T/R module has been successfully completed and transferred to production.

Table 1. HPA Performance
(includes circulator on output)

Key Parameters	Average performance of 500 HPAs
Input Dynamic Range	3.5dB
Gain	26.1dB
Peak Output Power	407W,
Efficiency	29.4%,
Waveform: Risetime	225ns,
Falltime	70ns,
Droop	0.25dB,
Phase across the pulse	<50°
Phase Linearity	±9 deg.max
Insertion Phase over Frequency	±50 deg.max
Spurious Rejection (f_o±100 to 350Mhz)	<80dBc
Transistor Junction Temp (Tj max)	<135°C@ worse ambient

Table 2. LNA/Switch Performance

Key Parameters	Average performance of 500 units
Receive: Noise Figure	2.2dB,
Gain	34.0dB,
Phase Tracking	< ± 8 deg.
VSWR	<1.4:1
Transmit:Insertion Loss	1.05dB,
Isolation	39dB,
VSWR	<1.25:1
Phase Track (4 path:)	± 3 deg.

Table 3. L-Band T/R Module Performance

Parameters	Average Performance of 500 modules
Transmit	
(PW=95µs,D.C=10%)	
Pout (avg.over freq)	>280W
Gain Track	<.35dB RMS (@worst freq)
Phase Track	<10°RMS (@worst freq)
Pin(DC)	140-180W
Risetime	<285ns
Amplitude Droop	<.35dB
ΔPhase (across pulse)	49° max
ΔPhase from Linear	± 9° max
Harmonics-(2nd & 3rd)	<80dBc
Spurious Signals	<80dBc
Pulse/Pulse Stability (70dBc Cancellation)	
Amplitude	<.06%
Phase	<.018°
Receive	
Gain	>32.7dB
Gain Track	<0.35dB RMS (@worst freq)
Phase Track	<5.0° RMS (@worst freq)
Noise Figure	<2.8dB
Pulse/Pulse Stability (70dBc Cancellation)	
Amplitude	<.06%
Phase	<.018°

ACKNOWLEDGEMENT

The authors would like to thank J. Kelly for his efforts in testing the devices and modules during the development of this program.